WHITE PAPER

Multi-Protocol Framer Design

Abstract:

Commonly used telecom protocols like E1, E2, E3, T1, T2, T3 etc. are very different from each other in terms of frame length, framing pattern, sequence, control channels, alarms and errors etc. Hence each of these protocols calls for a separate interfacing hardware design and protocol specific framers. Yet they are similar in more than one way, each one of them is in the form of a serial bit-stream with periodically repeating framing sequence. KritiKal has designed a multi-protocol framer design in VHDL, exploiting this similarity of popular telecom protocols. It can support any existing serial communication protocol and is field upgradeable to support newer protocols. This paper presents an overview of the design.

Design Overview

Most communication protocols have synchronization pattern, which is used for synchronization, and locking onto the bit-stream. The Multi-protocol framer design exploits this fact and is capable of implementing framing protocols for all such patterns, of different lengths (from 2 bits to 64Kbytes).

There are two components to the design. Hardware Component which is implemented in VHDL and stays same across all protocols; and a Firmware Component which is a mix of Assembly and C languages and which captures the differences among various protocols. The two components are briefly described below:

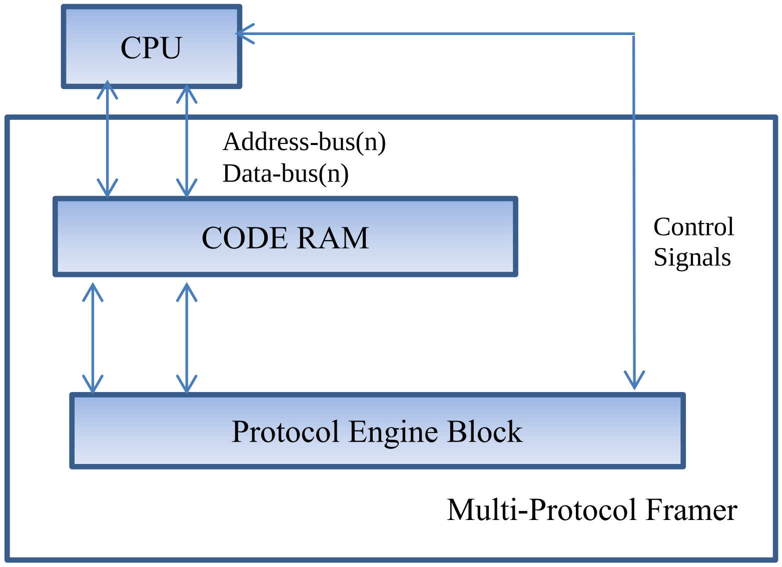
- **Hardware Component:** Any typical microcontroller has an instruction cache and a logic unit. Instruction cache stores the set of instructions and the logic unit executes the instructions. The programmer can load different sets of instructions to realize different functionalities. The multi-protocol framer design is based on this microcontroller architecture.

  It is implemented in two parts:

  - Code RAM Block
  - Protocol Control Engine

    ✓ **Code RAM** is used as the instruction cache. Protocol Control Engine reads and executes instructions from code RAM. The design has a proprietary instruction set. The instruction set is similar to a typical microprocessor like Arm, 8051, x86, PPC etc. The machine language code specific to the desired protocol is converted to a binary by an external utility (also part of the design) and loaded into the code RAM. The code RAM consists of a number of dual-port rams. The instructions are written into the code RAM by primary processor, and read by the protocol control engine. The code RAM is implemented as an asynchronous read, synchronous write, SRAM Block.

    ✓ **Protocol Control Engine** is responsible for the frame synchronization of the data stream for each of the various protocols. It detects the frame boundaries, under the control of a program describing the protocol being processed. The protocol control engine provides a generic interface which can implement any standard/proprietary protocol.



- **Firmware Component**: The firmware component is the program which captures the differences between various serial protocols. This is written in a sort of Assembly Language. The set of instructions that defines the framing of the desired protocol are referred to as proto-progs henceforth. These proto-progs are compiled into a binary and loaded in the code RAM during operation. The framer can be configured for different protocols, just by changing the proto-prog.

Applications:

1. High density Internet E1/E2/E3/T1/T2/T3 interfaces for multiplexers, switches, routers, and digital modems.
2. Frame Relay Switches and Access Deices
3. Digital Access and Cross-Connect Systems
4. PDH Add / Drop Multiplexers (ADMs)

Advantages:

1. Support for Multiple protocols in a single hardware.
2. It can be configured to support proprietary and non-standard protocols as well.
3. Brings field upgradeability to the product.
4. Enormous reduction in time to market by accelerating development and debugging cycles.
5. Reduced total cost of ownership.

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